PATENT APPLICATION

LOW VOLTAGE ANTIFUSE DEVICE AND PROCESS

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LOW VOLTAGE ANTIFUSE DEVICE AND PROCESS

BACKGROUND OF THE INVENTION

### 1.	Field of the Invention

5	The present invention relates to processes involved in the manufacturing of semiconductor devices on a substrate. More particularly, the present invention relates to new methods for forming antifuses on semiconductor wafers.

### 2.	Description of the Related Art

Integrated circuit devices are commonly designed with redundant components 10	such that a redundant component may be substituted for a defective component discovered during testing. For example, portions of a defective memory array may be repaired by substituting a redundant memory array for the defective one. Using this method, the yield or acceptable rate of chips produced on a wafer may be increased.

Conventional DRAM and SRAM memories often use laser fuse blowing 15	techniques, i.e., blowing one or more fuses with a laser beam to deactivate a defective cell or line. The unblown fuse has a low resistance whereas the blown fuse has a high resistance, typically functioning as an open circuit. But laser techniques are expensive and time consuming. Moreover, the laser energy can damage adjacent areas.

To address these issues, antifuse technology has been introduced. Antifuses 20	typically functionally present an open circuit when unblown, having relatively high resistances (e.g., several mega ohms or more) and relatively low resistances (usually

less than 1000 ohms) when blown. Both the fuses and the antifuses may be used to provide one-time programming capability to a circuit.

Antifuses are formed by one of several conventional methods using doped polysilicon layers. For example, according to a first conventional method, an oxide

5   layer is positioned between a first doped polysilicon or metal layer and a second doped polysilicon or metal layer. Typically these antifuse layers are approximately 100 Angstroms thick and require a high voltage to breakdown. For example, such antifuse devices are often located in FPGA's and require an applied electrical voltage of between 10 and 20 volts to activate the antifuse element. Activation in the antifuse

10   context refers to the step of implementing the redundant circuit.

According to a second conventional method, an antifuse element is formed in a doped polysilicon layer, the application of a high (i.e., well above nominal design voltage) converting the high resistivity polysilicon link to a low resistivity type.

Another conventional method places a thin (i.e., 15-25 Angstrom) silicon

15   oxide dielectric layer between conductive electrodes. Charge pumps are used to step up the circuit voltage to about 8 to 10 volts. However, the thin oxide layer often has a very high rate of leakage. Moreover, a large part of the area of the die is consumed by the charge pump.

As described, each of the conventional methods for forming antifuses has

20   certain drawbacks which affect their suitability for semiconductor applications. For each of them, special design considerations, such as including additional circuitry affect the design process, the size of the die, and special requirements such as

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additional power supply voltages. Accordingly, what is needed is a new method for

forming an antifuse that can be easily incorporated into CMOS process flow. That is,

not too thick or thin a dielectric layer and a low enough activation voltage to eliminate

the charge pump.

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SUMMARY OF THE INVENTION

To achieve the foregoing, the present invention provides methods for forming antifuses in a conventional CMOS process flow. By incorporating one additional implant step, an antifuse is created which has more desirable breakdown voltage

5   characteristics as compared to conventional antifuses.

In accordance with one embodiment of the present invention, an antifuse is created with a customized oxide thickness. The method of forming an antifuse on a semiconductor substrate includes providing a partially fabricated semiconductor device. Nitrogen is implanted into a first portion of the substrate of the partially

10   fabricated semiconductor device in a region unprotected by a photoresist mask. A dielectric oxide layer is grown on the nitrogen implanted substrate using a wet oxidation process. A gate material is deposited directly on the oxide layer, wherein the gate material comprises one terminal of the antifuse.

These and other features and advantages of the present invention are described

15   below with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1F illustrate the stages in formation of an antifuse in accordance with one embodiment of the present invention.

FIGS. 2A-2E illustrate the stages in formation of an antifuse and multiple gate oxides in accordance with an alternative embodiment of the present invention.

FIGS. 3A-3B are plots illustrating charge-to-breakdown for large area capacitors grown in nitrogen implanted substrates using wet and dry oxidation.

FIG. 4 is a plot illustrating time-to-failure under different stress conditions on nitrogen implanted surfaces.

FIGS. 5A-5B are plots illustrating current behavior for N and P channel transistors in accordance with one embodiment of the present invention.

FIG. 6 is a circuit implementation of an antifuse in accordance with one embodiment of the present invention.

FIG. 7 illustrates a sample behavior of the drain and gate current of a transistor formed in accordance with embodiments of the present invention

FIG. 8 illustrates a sample behavior of the voltage at the gate node of an antifuse formed in accordance with embodiments of the present invention

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the invention. Examples of the preferred embodiments are illustrated in the

5 accompanying drawings. While the invention will be described in conjunction with these preferred embodiments, it will be understood that it is not intended to limit the invention to such preferred embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims. In the following

10 description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. The present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

15 FIGS. 1A-1F illustrate the stages in formation of an antifuse in accordance with one embodiment of the present invention. Initially, a sacrificial oxide layer 104 is formed on the silicon substrate 102 in accordance with conventional process steps to protect the substrate from implantation damage. The sacrificial oxide layer may be of a conventional thickness, for example 50 to 300 Angstroms. Conventional methods

20 include, for example, thermal growth or chemical vapor deposition processes. Active regions of the substrate are shown separated by isolation areas 103, formed by methods well known to those of skill in the relevant arts.

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Next, as illustrated in FIG. 1B, a resist layer is formed on the partially fabricated wafer stack and patterned and etched to form a mask 106, preferably using conventional photolithography steps, to form open areas to receive a nitrogen implant of the desired dose. That is, the photoresist mask is formed on the wafer stack to

5   expose the anitfuse areas and to protect the remaining portions of the partially fabricated wafer stack from the implant. Standard processing steps may be used to form wells and diffusion areas (not shown) at appropriate locations on the substrate.

As illustrated in FIG. 1C, nitrogen 110 is implanted into the substrate. Preferably, the nitrogen implant comprises the normal isotope of nitrogen (N14) and

10   the implant dose falls within the range of about 5×10^{13} atoms/cm^2 to 1×10^{15} atoms/cm^2 of nitrogen at an energy preferably in the range from about 5 to 50 Kev. More preferably, the nitrogen implant dose is about 4×10^{14} atoms/cm^2 implanted at an energy of about 25 Kev. The nitrogen is implanted through conventional methods such as are well known to those of skill in the relevant art. In accordance with one

15   embodiment, the nitrogen is preferably implanted within 200-600 Angstroms of the interface between the sacrificial oxide and the substrate. The depth of the nitrogen implant is dependant upon the implantation energy and sacrificial oxide thickness. Following implantation, the resist is removed by conventional process steps, for example, by ashing and stripping. Next, preferably, a pre gate oxidation wet clean is

20   performed, again according to conventional techniques.

Next, as illustrated in FIG. 1D, a gate or sacrificial oxide is formed in a wet ambient 112. That is, the ambient is preferably provided with a uniform and

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controllable quantity of steam. Growth of the gate dielectric on a nitrogen implanted surface in a controllable wet ambient (i.e., wet or steam oxidation) creates insulating elements and atomic bonds that exhibit an enhanced and highly uniform rate of electrical wearout at lower voltages or times in comparison to gate dielectrics grown in dry or dry with HCl ambients to the same thickness. FIG. 1D illustrates the wet ambient 112 in the process of forming the oxide over the implanted nitrogen 114 formed in the silicon substrate 102.

The oxide is preferably grown at temperatures in the range from 750 to 1000 degrees C, more preferably from 800 to 900 degrees C. Beyond this range the process is not readily controllable. Suitable ambient temperatures may be provided by any suitable means as known to those of skill in the art, for example, including horizontal, vertical or rapid thermal furnaces. FIG. 1E illustrates the dielectric oxide layer 116 formed in the wet ambient. Under identical conditions, wet oxidation results in a higher growth rate than dry oxidation. That is, without wishing to be bound by any theory, it is believed that at high temperatures, H_2O dissociates into H and OH. The OH radicals diffuse faster in SiO_2 than O_2. Moreover, at the higher temperatures, the chemical reaction rate between oxygen (from the OH radicals) and silicon is higher.

By varying the conditions of ion implantation, for example the dose and energy, in combination with a wet oxidation ambient, the resulting final thickness of the oxide layer (i.e., the dielectric) can be engineered to produce a dielectric with high uniformity in thickness and low breakdown voltage when subjected to high electric fields. Preferably, the oxide dielectric 116 will have a thickness in the range of 30 to

40 Angstroms, more preferably about 35 Angstroms. The optimal thickness of the oxide dielectric 116 is dependant upon the distribution of N_2 in the oxide and the desired operating voltage. For example, while a thin oxide in the 30 to 40 Angstrom range is suitable for operating voltages of 1.8 V, an oxide dielectric thickness of 40 to

5   60 Angstroms is more suitable for higher operating voltages, such as at 2.5 volts.

Next, as illustrated in FIG. 1F, gate material is deposited and patterned and etched to form gate 118 in accordance with conventional CMOS process steps. For example, the gate may comprise polysilicon. Gate 118 serves as one terminal of the antifuse 120, an initially "open" link between the gate 118 and the substrate 102

10   converted to a conducting link to ground with the application of a suitably high voltage. That is, the present invention in one embodiment provides an antifuse, capable of detection by evaluating the effect of gate leakage on the gate node voltage. Further details as to the circuit implementation and detecting techniques are described below and illustrated with reference to FIG. 6.

15   In an alternative embodiment, the present invention may be combined with nitrogen implantation schemes for creating gates of multiple thicknesses in semiconductor devices. That is, after implanting the nitrogen into the antifuse region and in the regions underlying the transistor gates, an integrated circuit having gate oxides of one or more thicknesses is formed in conjunction with the antifuse. The

20   overall steps in the process in accordance with one embodiment are illustrated in FIGS. 2A – 2E.

In one embodiment, gate oxides are grown by first implanting a first portion of the semiconductor substrate with a first dose of an oxide growth retardant, for example nitrogen, implanting a second portion of the semiconductor substrate with a second dose of an oxide growth retardant for the formation of an antifuse, and lastly

5   oxidizing the semiconductor substrate in a first wet environment to grow a first oxide on the first portion and a second oxide on the second portion. Usually, a third portion of the semiconductor substrate is not implanted with any oxide growth retardant so that a third oxide is grown on the third portion during the common wet oxidation step. The third oxide is the thickest of the three. Thus, the method of forming an antifuse

10   by nitriding the substrate may be incorporated into the multiple gate process flow.

FIG. 2A is a cross-sectional view of an exemplary partially fabricated wafer 200 in which four filled isolation trenches 205, 210, 215, and 220 define three different islands (or active areas) 230, 235, and 240 where different technology node transistors operating at different operating voltages (Vdd) can be formed. In area 235,

15   an antifuse is formed in accordance with the steps described in FIGS. 1A-1C, the antifuse region preferably oxidized in a wet environment at the same time as the oxide layers for the transistors in regions 230 and 240.

Each transistor formed in areas of 230 and 240 can potentially represent a device of a different generational node. That is, because of the different operating

20   voltage (Vdd), each island of 230 and 240 requires a different gate oxide thickness. For example, the highest Vdd transistor built in 240 requires about 62Å of oxide, whereas the low Vdd transistor in 230 requires about 50Å of oxide.

It will be appreciated by those skilled in the art that although the exemplary wafer 200 is shown with three thicknesses of gate oxides, the particular requirements of the final product will dictate how many different thicknesses of gate oxides are required. Additionally, although many applications will require gate oxides that

5   correspond to generational nodes, other applications may require half-nodes or other non-standard oxide thicknesses.

Initially, as illustrated in FIG. 2B, a photo resist layer is deposited and patterned to form mask 250. The mask is designed to expose only the low thickness gate-oxide antifuse area 235 on the semiconductor substrate. The low thickness gate

10   oxide antifuse region 235 is then implanted with a high dose of an oxide growth retardant, for example a nitrogen implant 260. FIG. 2B is a cross sectional view of the exemplary wafer 200 during high dose implantation. The mask 250 covers the thickest oxide area 240 and the low voltage transistor region 230, exposing only the antifuse gate oxide area 235 so that nitrogen 260 will only be implanted in area 235.

15   The nitrogen implant for the antifuse is performed in accordance with the techniques described in FIGS. 1A-1E. That is, preferably, the nitrogen implant comprises the normal isotope of nitrogen (N14) and the implant dose falls within the range of about 5 x 10^{13} atoms/cm^2 to 1 x 10^{15} atoms/cm^2 of nitrogen at an energy preferably in the range from about 5 to 50 Kev. More preferably, the nitrogen implant

20   dose is about 4 x 10^{14} atoms/cm^2 implanted at an energy of about 25 Kev. The nitrogen is implanted through conventional methods such as are well known to those of skill in the relevant art. By varying the conditions of ion implantation, for example

the dose and energy, in combination with a wet oxidation ambient, the resulting final thickness of the oxide layer (i.e., the dielectric) can be engineered to produce a dielectric with high uniformity in thickness and low breakdown voltage when subjected to high electric fields. Preferably, the oxide dielectric for the antifuse in

5 region 235 will have a thickness in the range of 30 to 40 Angstroms, more preferably about 34 to 35 Angstroms. The optimal thickness of the oxide dielectric is dependant upon the distribution of N_2 in the oxide and the desired operating voltage.

Referring back to FIG. 2B, after implantation the mask is removed. The removal can be accomplished with standard resist strip processes. For example, either

10 a wet or dry etch clean can be used, as appropriate.

Next, as illustrated in FIG. 2C, a photo resist layer is deposited and patterned to form mask 255. The mask is designed to expose only the low thickness gate-oxide area 230 on the semiconductor substrate. The low thickness gate oxide region 230 is then implanted with an appropriate dose of an oxide growth retardant, for example a

15 small dose of nitrogen 280. The mask 255 exposes only the thin gate oxide area 230 so that the correct dose of nitrogen 280 will only be implanted in that the area 230. After implantation the mask is removed in accordance with the techniques described above. The dosage of nitrogen required in this and the following steps varies with the final gate oxide thicknesses required for the transistors. By controlling dosage and

20 exposure times in accordance with techniques known to those of skill in the art, the nitrogen implants can be used to grow gate oxides of various thicknesses in a single oxidation step.

Next, as illustrated in FIG. 2D, a photo resist layer is deposited and patterned to form mask 259. The mask is designed to expose the high thickness gate-oxide area 240 on the semiconductor substrate as well as the low thickness gate-oxide area in region 230. The high thickness gate oxide region 240 and the low thickness region 230 is then implanted with an appropriate dose of an oxide growth retardant, for example a dose of nitrogen 290. The mask 259 exposes the thick gate oxide area 240 so that the correct dose of nitrogen 290 will be implanted in the area 240 and a supplemental implant of nitrogen will occur to the already nitrided region 230. These steps could be repeated as many times as necessary for different thicknesses of oxides. It should be noted that in an alternative embodiment, the exemplary wafer 200 of FIGS. 2A-2D, the thickest gate oxide area 240 is not implanted with any oxidation retardant. In yet another alternative embodiment, masking is performed so that only one region at a time is exposed. That is, according to this alternative embodiment, rather than accumulating nitrogen implants in a specific region in two or more implant steps or exposures, each region is unmasked only once and the amount of implanted nitrogen in that specific region determined only from a single implant step.

Once all the areas that require an oxide growth retardant are implanted, the sacrificial oxide is stripped. For example, a hydrofluoric acid clean, followed by an RCA clean, followed by a hydrofluoric clean would be appropriate. It is to be noted that it is preferred to keep the sacrificial oxide as thin as possible as a protection layer for masking and implant steps.

The oxides are then grown in a wet ambient 275 as illustrated in FIG. 2E. The conditions of growth are those previously contemplated when the oxide growth implantation steps were performed. That is, the ambient is preferably provided with a uniform and controllable quantity of steam. Growth of the gate dielectric on a

5   nitrogen implanted surface in a controllable wet ambient (i.e., wet or steam oxidation) creates insulating elements and atomic bonds that exhibit an enhanced and highly uniform rate of electrical wearout at lower voltages or times in comparison to gate dielectrics grown in dry or dry with HCl ambients to the same thickness. The oxide is preferably grown at temperatures in the range from 750 to 1000 degrees C, more

10   preferably from 800 to 900 degrees C. Suitable ambient temperatures may be provided by any suitable means as known to those of skill in the art, for example, including horizontal, vertical or rapid thermal furnaces.

FIG. 2E is a cross sectional view of the exemplary wafer 200 showing the oxide growth during wet oxidation. During growth, the implanted areas naturally

15   grow thinner due to the retarding effect of the nitrogen on oxidation. FIG. 2E is a cross sectional view of the exemplary wafer 200 with its final oxide growths 271, 272, and 273. That is, a thinner gate oxide 271 is grown in the low voltage transistor area 230 whereas a thicker gate oxide 273 is grown in the high voltage transistor area 240. As discussed above in reference to FIGS. 1A-1D, the gate oxide layer 272 for the

20   antifuse preferably has a thickness in the range of 30-40 Angstroms. More preferably, gate oxide 272 for the transistor functioning as the antifuse in region 235 has a thickness of about 34 to 35 Angstroms. The thicknesses of the oxides 271 and 273 in the regions 230 and 240 are dependant upon the desired operating voltages and the

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nitrogen implant procedure is preferably adjusted to achieve those oxide thicknesses in accordance with methods known to those of skill in the relevant arts. Thus, further description as to nitrogen implant ranges and corresponding gate oxide thicknesses formed in the wet oxidation steps are deemed unnecessary here.

5   FIGS. 3A-3B are plots illustrating cumulative charge-to-breakdown for large area capacitors grown in nitrogen implanted substrates using wet and dry oxidation. Charge-to-breakdown ("QBD") is a method used to determine the reliability of thin gate oxides in MOS devices. Typically, voltage is applied to the MOS structure to force a controlled amount of charge to breach the dielectric. As illustrated in FIG. 3A,

10   the N channel Charge-to-Breakdown values are shown for large area capacitors grown in $4 \times 10^{14}/cm^2$ nitrogen implanted surface using alternatively wet and dry oxidation. As shown, the devices characterized consistently resulted in a lower QBD for wet oxidation as compared to dry oxidation. The oxide thickness for the samples was about 34 Angstroms. This same relationship held for the P channel charge-to-

15   breakdown illustrated in FIG. 3B. Thus, as shown, the charge to breakdown for the oxide formed by wet oxidation techniques is significantly reduced (i.e., about 1/10th) in comparison to than that required for oxides formed by dry oxidation techniques. This enables dielectrics formed by the techniques of the present invention to convert from "open" links to conducting links at smaller applied voltages than typical

20   antifuses in the same time or conversely in a smaller time at the same voltage. Preferably, the breakdown or programming voltage is 5 volts or less at a very short programming time, although the invention is not so limited.

The antifuses produced by the techniques of the present invention also result

in lower programming times. FIG. 4 is a plot illustrating time-to-failure under

different stress conditions on a nitrogen implanted surface. Time-to-failure is also

known as time dependent dielectric breakdown (TDDB) and is the time needed to

5   break down an oxide stressed at a given electric field. The oxides (wet and dry) were

grown on a surface implanted with nitrogen at a dose of 4×10^{14} /cm^2. The time to

failure for the dry oxide 404 is about 200 times the time to failure for the wet oxide

402. For example, at an applied stress voltage of 4.75 V, the wet oxide breaks down

in a period under 15 seconds as compared to about 3000 seconds for the dry oxide.

10   The operation of the dielectric is not compromised at low voltages. That is, under low

voltage operating conditions (e.g 1-1.8V), these nitrided oxides still possess adequate

lifetimes. For example, the data presented in FIG. 4 may be extrapolated to indicate

that the low field breakdown voltage easily exceeds the 10-year operating lifetime

requirement.

15   The performance of the transistor at normal operating conditions is not

compromised either. FIGS. 5A-5B are plots illustrating current behavior of devices

produced by wet oxidation in comparison to conventional devices produces by dry

oxidation. FIG. 5A-5B illustrates the Ion-Ioff behavior for N and P channel

transistors having gate oxides produced by either wet or dry oxidation steps. As

20   shown, the drive currents for the wet and dry processes in the target length region 502

are comparable for the N channel transistors as are the respective drive currents in the

target length region 504 for the P channel transistors shown in FIG. 5B.

Controlling the gate oxide breakdown behavior of a FET transistor to implement antifuse functions requires special consideration. While not wishing to be bound by any theory, it is believed that after gate oxide breakdown the channel in the transistor continues to provide current. That is, the gate breaks down in one spot, but the undamaged gate areas continue to control the channel effectively. FIG. 7 illustrates a sample behavior of the drain and gate current of a transistor formed in accordance with embodiments of the present invention. Specifically, the Id/Vg and Ig/Vg behavior of a 11/0.18 NMOS transistor before and after gate oxide breakdown is illustrated. As shown by the drain current plots before and after oxide breakdown in the transistor, the device continues to perform well in spite of a substantial increase in gate leakage. Drain to Source conductance is still well controlled by the device.

Thus, in lieu of sensing a change in the drain to source conduction, the present invention in one embodiment uses the increase in gate leakage of the device as a signal. FIG. 6 is a circuit implementation of an antifuse sensing circuit in accordance with one embodiment of the present invention.

The programmed state of the device was implemented in HSPICE as a simple Voltage-Controlled-Current-Source (VCCS) whose current is modeled by the exponential curve fit to gate leakage shown in FIG. 8.

The antifuse 602 is formed by implanting nitrogen and growing an oxide in a wet ambient as described above with reference to FIGS. 1A-1F and 2A-2E. In other words, the antifuse 602 comprises a transistor that has a relatively low charge to breakdown when subjected to a high electrical field. FIG. 6 illustrates the antifuse

602 configured in a read or detection circuit 600. As known to those of skill in the relevant art, a separate "writing" or programming circuit is used to program the antifuse. In this case, programming involves increasing the gate oxide leakage of the antifuse 602 by applying a high voltage to the terminals, the high voltage damaging

5   the gate oxide and causing the significant increase in gate leakage.

The antifuse 602 includes a first node, i.e., the gate node 604, connected to a sense amp gate (not shown) to determine the state of the antifuse, i.e., whether it is in a "0" state (unprogrammed) or a "1" (programmed) state. The antifuse 602 includes drain, source, and substrate regions 606 which are all grounded. Access is provided

10   by the select transistor 616. The select device 616 is used to access the antifuse whose drain, source and substrate are all grounded. That is, when an input voltage (representing a digital "1") is applied to the gate 612 (i.e., the select word line) the select transistor 616 is turned "on" to supply a voltage (V_{DD}) to the antifuse gate node 604. When the antifuse is unprogrammed (i.e., erased or undamaged) the gate oxide

15   leakage in the antifuse 602 is minimal, for example on the order of 1.0×10^{-4} nA, such as illustrated as reference point 704 in FIG. 7. That is, when the access word line 612 sees a signal, during the unprogrammed or erased state the antifuse device 602 does not conduct any gate current, or at least negligible amounts. This allows the gate node 604 to rise to a high voltage value.

20   In contrast, when the antifuse 602 is programmed, the gate leakage in the antifuse 602 is significantly greater. For example, as illustrated in FIG. 7, the gate leakage current 702 at a gate voltage of approximately 1.0 volt is approximately 1.0 x

10^2 nA. The gate leakage current allows a high current connection to the antifuse 602 ground terminals 606, and thereby pulls the node 604 down to a low voltage value. Proper selection of the antifuse device length and widths can be used to maximize the difference in these two voltages for fast sensing. Since the same set of access and

5   sensing devices will be in the path during the "programming" phase, it is advisable to use thicker oxide devices (such as for the select transistor 616 and the sense amplifier) for additional margin (over the 200x lifetime difference).

FIG. 8 illustrates a sample behavior of the voltage at the gate node of an antifuse formed in accordance with embodiments of the present invention under

10   "programmed" and "erased" conditions. FIG. 8 shows the results of a simulation when the access word line sees a signal. That is, when the access word line 612 sees an input signal 802, the antifuse gate node 604 reaches a higher voltage 804 during erased conditions (when the gate oxide is intact) than the voltage 806 reached when the device is programmed (the oxide is damaged). Thus, according to one

15   embodiment, the antifuse detection circuit is configured with a gate node of the antifuse connected to a higher voltage node.

By implementing these techniques into the CMOS flow, antifuse elements may be created having highly uniform and controllable rates of wearout at lower voltages, and/or times in comparison to gate dielectrics grown by dry oxidation

20   processes or dry with HCl oxidation processes. The controllable low rate of wearout enables its use in a chip as a low voltage antifuse, thereby eliminating the need for

boosting voltages by charge pumps or alternatively reducing the number of charge pump stages.

Thus, lower programming voltages or times may be achieved without compromising the device lifetime at the operating voltages. For example, breakdown times at programming voltages of 5 V are less than 1 second compared to lifetimes of greater than 1000 years at the operating voltage of at the operating voltage of 1.8V. This antifuse technology provides further advantages over laser blowing techniques. For example, unlike laser blown fuse technology, the proposed scheme can be brought within the die thereby reducing die size. Moreover, the antifuses may be placed adjacent to the memory array provided that the programming voltages can be routed to the antifuse area. Thus, routing restrictions for metals within the repair bank are eliminated. The antifuses formed by the method of the present invention may also be used as one-time field programmable elements in additional applications.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.